Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.067”**

**.067”**

**B**

**E**

**E**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: COLLECTOR**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .067” X .067” DATE: 10/19/21**

**MFG: ZETEX THICKNESS .010” P/N: ZTX951**

**DG 10.1.2**

#### Rev B, 7/1